NIKOLAOS BELLAS

Curriculum Vitae

Associate Professor

University of Thessaly

Department of Computer and Communication Engineering	Phone: +30-24210-74704
University of Thessaly	Cell: +30-6947-724154
37 Glavani Str.	**Email**: nbellas@uth.gr
38221	**URL**: http://inf-server.inf.uth.gr/~nbellas
Volos, Greece	

Education

December 1998 **University of Illinois at Urbana-Champaign**, Ph.D. in Electrical and Computer Engineering,.
Dissertation Title: "*Architectural and Compiler Support for Energy Reduction in High Performance Microprocessors*". Advisors: Ibrahim Hajj and Constantine Polychronopoulos
G. P. A. = 5.0/5.0

May 1995 **University of Illinois at Urbana-Champaign**, M.Sc. in Electrical and Computer Engineering.
Thesis Title: "*A Novel Design for Testability Technique Using State Space Information*"
Advisor: Daniel Saab.
G. P. A. = 5.0/5.0

November 1992 **University of Patras, Greece,** Diploma in Computer Engineering and Informatics.
Emphasis on VLSI systems, Signal processing, and Computer Architecture.
G. P. A. = 9.15/10

Professional Experience

Fall 2007 – Present: Associate Professor, ECE Department, University of Thessaly, Volos, Greece

Fall 2007 – Spring 2008 : Consultant with Tensilica, Inc., Mountain View, CA
Ported the AVS video decoding standard to the Tensilica Diamond processor using Tensilica instruction extensions and dual core API.

Oct. 2001 – Spring 2007: Principal Staff Engineer, Embedded Systems Research., Motorola Inc., Schaumburg, IL

- Technical lead of a five-person team working on reconfigurable computing.

- Designed CAD tool that compiles streaming applications written in a high level language to accelerators in a System On FPGA platform.

- Chief architect of two ASIC chips that perform image processing for wireless multimedia applications for the next generation camera-enabled Motorola phones. The image sensor companion chips are used to perform image processing, sensor control, color space conversion, etc. I developed the RTL for the image processing chain of the chip, and part of the embedded software for the drivers of the modules.

- Participated in the design of a System On Chip ASIC design for an automotive application. The chip was based on the ARM9 RISC processor and a streaming co-processor to accelerate performance critical kernels. I wrote a cycle accurate simulator of the co- processor to be used for chip functional verification.

May 1999 – Oct. 2001: Senior Staff Engineer, Multimedia Architecture Lab, Motorola Inc., Schaumburg, IL

- Architect of a scalable, programmable architecture for MPEG4 video and JPEG image compression.

- Designed a programmable Motion Estimation module and defined an Instruction Set Architecture for motion estimation algorithms.

- Designed the image-processing module that interfaces to the image sensor and wrote a bit-exact functional model for the MPEG4 encoder for chip verification.

- Participated in chip hardware testing, and in the design and implementation of the image processing algorithms. The chip is used in Motorola's first 3G (Third Generation) camera cell phone.

Dec. 1998 - May 1999: Postdoctoral research associate, Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Champaign, IL

Summer 1996: Research Intern, Design Technology Labs, Intel Corp., Santa Clara, CA

Summer 1995: Research Intern, Silicon Graphics, Mountain View, CA

Peer Reviewed Publications

Journal Publications

J1. Vassilis Vassiliadis, Charalampos Chalios, Konstantinos Parasyris, Christos D. Antonopoulos, Spyros Lalis, Nikolaos Bellas, Hans Vandierendonck, Dimitrios S. Nikolopoulos. Exploiting Significance of Computations for Energy-Constrained Approximate Computing. *International Journal of Parallel Programming (IJPP).* pg. 1-21 March 2016.

J2. K. Krommydas, Wu-chun Feng, Christos D. Antonopoulos, and N. Bellas. OpenDwarfs: Characterization of Dwarf-Based Benchmarks on Fixed and Reconfigurable Architectures. *Journal of Signal Processing Systems. US* Springer. pg. 1-20. October 2015.

J3. M. Owaida, G. Falcao, J. Andrade, C. Antonopoulos, N. Bellas, M. Purnaprajna, D. Novo, G. Karakonstantis, A. Burg, and P. Ienne. Enhancing design space exploration by extending CPU/GPU specifications onto FPGAs. *ACM Transactions on Embedded Computing Systems (TECS).* March 2015.

J4. Dimitrios Nikolopoulos, Hans Vandierendock, Nikolaos Bellas, Christos D. Antonopoulos, Spyros Lalis, Georgios Karakonstantis, Andreas Burg, Uwe Naumann. Energy Efficiency through Significance-Based Computing. *IEEE Computer.* Vol. 47. Issue 7. Pg. 82-85. July 2014.

J5. Maria Koziri, Dimitris Zacharis, Ioannis Katsavounidis, Nikolaos Bellas . Implementation of the AVS Video Decoder on a Heterogeneous Dual-Core SIMD Processor. *IEEE Transactions on Consumer Electronics*, vol. 57, No. 2, pp. 673-681, May 2011.

J6. Seda Ogrenci Memik, Nikolaos Bellas, Somsubhra Mondal. Pre-synthesis Area Estimation of Reconfigurable Streaming Accelerators. *IEEE Transactions on Computer-Aided Design*, Volume: 27, No: 11, pp. 2027-2038, November 2008.

J7. Nikolaos Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier. Mapping streaming architectures on reconfigurable platforms. ACM SIGARCH Computer Architecture News. Volume 35 , Issue 3, Pages: 2 – 8, June 2007

J8. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos. Using dynamic cache management techniques to reduce energy in general purpose Processors. *IEEE Transactions on VLSI Systems*, Volume: 8, Issue : 6, pp. 693-708, December 2000.

J9. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos, George Stamoulis. Architectural and Compiler Techniques for Energy Reduction in High Performance Microprocessors. *IEEE Transactions on VLSI Systems, Special Issue on Low Power,* Volume:8, Issue:3, pp. 317-326, June 2000

J10. Amber-Roy Chowdhury, Nikolaos Bellas, Prithviraj Banerjee. Algorithm Based Error Detection Schemes for Iterative Solution of Partial Differential Equations. *IEEE Transactions on Computers*, pp. 394-407, Vol. 45, Number 4, April 1996

Conference and Workshop Publications

C1. Ioannis Parnassos, Panagiotis Skrimponis, Georgios Zindros, Nikolaos Bellas. SoCLog: A Real-Time, Automatically Generated Logging and Profiling Mechanism for FPGA-based Systems On Chip. *26th International Symposium on Field Programmable Logic and Applications (FPL).* August 28 – September 2, 2016. Lausanne, Switzerland.

C2. Vassilis Vassiliadis, Jan Riehme, Jens Deussen, Konstantinos Parasyris, Christos D. Antonopoulos, Nikolaos Bellas, Spyros Lalis and Uwe Naumann. Towards Automatic Significance Analysis for Approximate Computing. *International Symposium on Code Generation and Optimization (CGO).* March 14-16, 2016. Barcelona, Spain.

C3. Vassilis Vassiliadis, Charalampos Chalios, Konstantinos Parasyris, Christos D. Antonopoulos, Spyros Lalis, Nikolaos Bellas, Hans Vandierendonck, Dimitrios S. Nikolopoulos. A Significance-Driven Programming Framework for Energy-Constrained Approximate Computing. *ACM International Conference on Computing Frontiers.* May 18-21, 2015. Ischia, Italy.

C4. Konstantinos Parasyris, Vassilis Vassiliadis, Christos D. Antonopoulos, Spyros Lalis and Nikolaos Bellas. A Significance-Aware Software Stack for Computing on Unreliable Hardware. *Second Workshop on Approximate Computing Across the System Stack (WACAS).* March 15, 2015. Istanbul, Turkey.

C5. Konstantinos Parasyris, Georgios Tziantzioulis, C.D. Antonopoulos, Nikolaos Bellas. GemFI: A Fault Injection Tool for Studying the Behavior of Applications on Unreliable Substrates. *International Conference on Dependable Systems and Networks (DSN).* June 23-26, 2014. Atlanta, GA

C6. Konstantinos Krommydas, Wu-Chun Feng, Muhsen Owaida, Christos D. Antonopoulos and Nikolaos Bellas. On the Portability of OpenCL Dwarfs on Fixed and Reconfigurable Parallel Platforms. *25th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP).* June 18-20, 2014, Zurich, Switzerland. **(Nominated for Best Paper Award).**

C7. Muhsen Owaida, Christos D. Antonopoulos, Nikolaos Bellas. A Grammar Induction Method for Clustering of Operations in Complex FPGA Designs. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Regular paper.* May 11-13, 2014. Boston, MA

C8. Gabriel Falcao, Muhsen Owaida, David Novo, Madhura Purnaprajna, Nikolaos Bellas, Christos D. Antonopoulos, Georgios Karakonstantis, Andreas Burg and Paolo Ienne. Shortening design time through multiplatform simulations with a portable OpenCL golden-model: the LDPC decoder case. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, April-May 2012. Toronto, ON.

C9. Muhsen Owaida, Nikolaos Bellas, Christos Antonopoulos, Konstantis Daloukas, Charalambos Antoniadis. Massively Parallel Programing Models Used as Hardware Description Languages: The OpenCL Case. *International Conference on Computer-Aided Design (ICCAD),* November 6-10, 2011, San Jose, CA

C10. Konstantinos Krommydas, Wu-Chun Feng, Christos Antonopoulos, Nikolaos Bellas. AVS Video Decoder on Multicore Systems: Optimizations and Tradeoffs. *In Proceedings of the 2011 International Conference on Multimedia and Expo (ICME) – Industrial Program*, July 2011, Barcelona, Spain.

C11. Georgios Karakonstantis, C.D. Antonopoulos, Nikolaos Bellas, Kaushik Roy. Significance Driven Computation on Next Generation Unreliable Platforms. *Design Automation Conference (DAC), Wild And Crazy Ideas Session (WACI)*, June 5-10, 2011, San Diego, CA

C12. Kostas Theocharoulis, Haralambos Antoniadis, Nikolaos Bellas, C.D. Antonopoulos. Implementation and Performance Analysis of Seal Encryption on FPGA, GPU, and Multicore Processors. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 1-3, 2011, Salt Lake City, UT

C13. Muhsen Owaida, Nikolaos Bellas, Konstantis Daloukas, Christos D Antonopoulos. Synthesis of Platform Architectures from OpenCL Programs. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 1-3, 2011, Salt Lake City, UT

C14. Konstantis Daloukas, C.D. Antonopoulos, Nikolaos Bellas. GLOpenCL: OpenCL Support on Hardware- and Software-Managed Cache Multicores. *6th International Conference on High Performance Embedded Architectures & Compilers (HiPEAC).* January 24-26, 2011, Heraklion, Greece.

C15. Konstantinos Krommidas, Georgios Tsoublekas, C.D. Antonopoulos, Nikolaos Bellas. Mapping and Optimization of the AVS Video Decoder on a High Performance Chip Multiprocessor. *International Conference on Multimedia and Expo (ICME),* July 19-23, 2010, Singapore.

C16. Konstantis Daloukas, C.D. Antonopoulos, Nikolaos Bellas, Sek M. Chai. Fisheye Lens Distortion Correction on Multicore and Hardware Accelerator Platforms. 24th *International Parallel and Distributed Processing Symposium (IPDPS), A*pril 19-23, 2010, Atlanta, GA

C17. Sek M. Chai, Nikolaos Bellas, Abelardo Lopez Lagunas. Extending a Stream Programming Paradigm to Hardware Accelerator Platforms. *Symposium on Application Accelerators for High Performance Computing (SAAHPC 2009),* July 27-31 2009, Champaign, IL

C18. Nikolaos Bellas, Ioannis Katsavounidis, Maria Koziri, Dimitris Zacharis. Mapping the AVS Video Decoder on a Heterogeneous Dual-Core SIMD Processor. *46th Design Automation Conference (DAC)-User Track.* July 26-31, 2009, San Francisco, CA

C19. Konstantis Daloukas, C.D. Antonopoulos, Nikolaos Bellas. Implementation of a Wide-angle Lens Distortion Correction Algorithm on the Cell Broadband Engine. 23rd *International Conference on Supercomputing (ICS),* June 8-12, 2009, New York Metro Area, NY

C20. Nikolaos Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier. Real-Time Fisheye Lens Distortion Correction Using Automatically Generated Streaming Accelerators. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, April 5-7, 2009, Napa Valley, CA

C21. Nikolaos Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier. An Architectural Framework for Automated Streaming Kernel Selection. 14th *Reconfigurable Architectures Workshop (RAW),* March 2007, Long Beach, CA

C22. Nikolaos Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier. Mapping Streaming Architectures on Reconfigurable Platforms. *Reconfigurable and Adaptive Architectures Workshop (RAAW), in conjunction with Micro*, December 10th, 2006, Orlando, FL

C23. Sek Chai, Nikolaos Bellas, Greg Kujawa, Tom Ziomek, Linda Dawson, Tony Scaminaci, Malcolm Dwyer, Dan Linzmeier. Reconfigurable Streaming Architectures for Embedded Smart Camera Applications. *2nd IEEE Workshop on Embedded Computer Vision, in conjunction with CVPR,* June 18, 2006, New York, NY

C24. Nikolaos Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier. FPGA implementation of a license plate recognition SoC using automatically generated streaming accelerators. 13th *Reconfigurable Architectures Workshop (RAW),* 25-26 April 2006, Rhodes, Greece

C25. Sek Chai, Nikolaos Bellas, Malcolm Dwyer, Dan Linzmeier. Stream Memory Subsystem in Reconfigurable Platforms. 2nd *Workshop on Architecture Research using FPGA Platforms (WARFP),* February 12, 2006, Austin, TX

C26. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos, George Stamoulis. Energy and Performa Improvements in Microprocessor Design using a Loop Cache. *Proceedings of the International Symposium on Computer Design (ICCD)*, pp. 378-383, October 1999, Austin, TX

C27. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos. Using dynamic cache management techniques to reduce energy in a high-performance microprocessor. *International Symposium of Low Power Electronics and Design (ISLPED),* pp. 64-69, August 1999, San Diego, CA

C28. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos. A detailed, transistor-level energy model for SRAM-based caches. *International Symposium of Circuits and Systems (ISCAS)*, Volume:6, pp.198-201, June 1999, Orlando, FL

C29. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos, George Stamoulis. Architectural and Compiler Support for Energy Reduction in the Memory Hierarchy of High Performance Microprocessors. *Proceedings of the International Symposium of Low Power Electronics and Design (ISLPED*), pp. 70-75, August 1998, Monterey, CA

C30. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos, George Stamoulis. A new scheme for I-Cache energy reduction in High Performance Processors. *Power-Driven Microarchitecture Workshop, International Symposium On Computer Architecture (ISCA),* June 1998, Barcelona, Spain

Poster presentations

C31. Vassilis Vassiliadis, Konstantinos Parasyris, Charalampos Chalios, Christos D. Antonopoulos, Spyros Lalis, Nikolaos Bellas, Hans Vandierendonck, Dimitrios S. Nikolopoulos. A programming model and runtime system for significance-aware energy-efficient computing. *ACM SIGPLAN 20th Symposium on Principles and Practice of Parallel Programming (PPoPP*). February 9-11, 2015. San Francisco, CA

C32. Muhsen Owaida, Christos D Antonopoulos, Nikolaos Bellas, Konstantis Daloukas, Charalambos Antoniadis, Konstantinos Krommidas, Georgios Tsoublekas,. Implementation and Performance Comparison of the Motion Compensation Kernel of the AVS Video Decoder on FPGA, GPU and Multicore Processors. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 1-3, 2011, Salt Lake City, UT

C33. Nikolaos Bellas, Sek M. Chai, Malcolm Dwyer, Dan Linzmeier, Abelardo Lopez Lagunas. Proteus: An Architectural Synthesis Tool based on the Streaming Programing Model. *19th International Conference on Field Programmable Logic and Applications (FPL)*, August/September 2009, Prague, The Czech Republic

C34. Somsubhra Mondal, Seda O. Memik, Nikolaos Bellas. Pre-synthesis area estimation of reconfigurable streaming accelerators. *16th International Conference on Field Programmable Logic and Applications (FPL)*, August 28-30 2006, Madrid, Spain

C35. Nikolaos Bellas, Arnold Yanof. An Image Processing Pipeline with Digital Compensation of Low Cost Optics for Mobile Telephony. *International Conference on Multimedia and Expo (ICME)*, July 9-12, 2006, Toronto, Canada

C36. Nikolaos Bellas, Sek M. Chai, Malcolm Dwyer, Dan Linzmeier. Template-based generation of streaming accelerators from a high level representation. *International Symposium on Field-Programmable Custom Computing Machines (FCCM),* April 24-26, 2006, Napa Valley, CA

C37. Somsubhra Mondal, Seda O. Memik, Nikolaos Bellas. Pre-synthesis Queue Size Estimation of Streaming Data Flow Graphs. *International Symposium on Field-Programmable Custom Computing Machines (FCCM),* April 24-26, 2006, Napa Valley, CA

C38. Nikolaos Bellas, Malcolm Dwyer. A programmable, high performance Vector array unit used for Real-time Motion Estimation. *Proceedings of the International Conference on Multimedia and Expo (ICME)*, Volume: 1, pp.117-120, July 2003, Baltimore, MD

Other publications

Nikolaos Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier. " A Multi-channel DMA module for streaming computations". IP.com Prior Art Database, IPCOM000133577D.

Tutorials, Invited Talks, Panels

September 2016: Approximate computing for next generation platforms. ARM Research Summit. Cambridge, UK.

March 2016: Reliability and Energy-efficiency optimizations using Significance-Based Computing. Keynote Talk in Workshop on Parallel Programming for Resilience and Energy Efficiency (PP4REE). Barcelona, Spain.

March 2015: Panel: Enablers and Roadblocks for Mainstream Adoption of Approximate Computing Paradigm. In conjunction with WACAS 2015. Istanbul, Turkey.

October 2014: Significance-Based Computing for Reliability and Power Optimization. HiPEAC Computing Systems Week. Athens, Greece.

May 2014: "Significance-Based computing". Aristotle University of Thessaloniki, GR.

May 2012: "Massively Parallel Programming Models Used as Hardware Description Languages: The OpenCL Case". University of Toronto, Toronto, ON.

August 2011: "Massively Parallel Programming Models Used as Hardware Description Languages: The OpenCL Case". Stanford Research Institute (SRI), Princeton, NJ.

March 2007: "Automatic Generation of Streaming Accelerators from a High Level Representation". Department of Electrical Engineering, University of California at Riverside, CA.

September 2006: "Programming models and Architectures for Reconfigurable Platforms". Motorola Software, Systems, Simulation (S3) Symposium, Itasca, IL

March 2006: "Programming Models and Architectures for FPGAs". Motorola Symposium on Innovations in DSP and Embedded Systems Design using FPGAs, Schaumburg, IL

September 2005: "Automatic Generation of Imaging Architectures from an Algorithmic Representation". Motorola Software, Systems, Simulation (S3) Symposium, Itasca, IL

June 2003: " Imaging Technologies at Motorola Labs", Computer Engineering and Informatics Department, University of Patras, Greece

February 2000: "Loop-Cache: An Instruction Hierarchy Component for Reduced Energy Consumption". Department of Electrical and Computer Engineering, Northwestern University, Evanston, IL

September 1999: "Architectural and Compiler Techniques for Energy Reduction in High Performance Processors". Department of Electrical and Computer Engineering, Purdue University, W. Lafayette, IN

December 1998: "Architectural and Compiler Techniques for Energy Reduction in High Performance Processors". IBM Research, Austin, TX

November 1998: "Architectural and Compiler Techniques for Energy Reduction in High Performance Processors". Microprocessor Research Labs, Intel Corp. Portland, OR

August 1996: "Novel techniques for Power reduction in High Performance Processors ". Design Technology Labs, Intel Corp., Santa Clara, CA

Citations

Approximately 850 citations.
H-Index = 14

Patents

P1. **US Patent 8,855,441** Sek M. Chai, Malcolm Dwyer, Dan Linzmeier, Ruei-Sung Lin, Nikolas Bellas. "Method and apparatus for transforming a non-linear lens-distorted image", October 2014, Motorola Corp.

P2. **US Patent 8,326,077** Sek M. Chai, Malcolm Dwyer, Dan Linzmeier, Ruei-Sung Lin, Nikos Bellas. "Method and apparatus for transforming a non-linear lens-distorted image", December 2012, Motorola Corp.

P3. **US Patent 7,802,005** Sek M. Chai, Nikos Bellas, Malcolm Dwyer, Dan Linzmeier. "Method and apparatus for configuring buffers for streaming data transfer". September 2010, Motorola Corp.

P4. **US Patent 7,683,948** Arnold Yanof, Nikos Bellas. "System and method for bad pixel replacement in image processing". March 2010, Freescale Corp.

P5. **US Patent 7,603,492** Sek M. Chai, Nikos Bellas, Malcolm Dwyer, Erica Lau, Zhiyuan Li, Dan Linzmeier. "Automatic generation of streaming data interface circuit ", October 2009, Motorola Corp.

P6. **US Patent 7,580,070** Arnold Yanof, Nikos Bellas**.** "System and method for roll-off correction in image processing", August 2009, Freescale Corp.

P7. **US Patent 7,441,224,** Nikos Bellas, Sek M. Chai, Dan Linzmeier. "Streaming kernel selection for reconfigurable processor", October 2008, Motorola Corp.

P8. **US Patent 7,305,649,** Nikos Bellas, Sek Chai, Erica Lau, Zhiyuan Li, Dan Linzmeier. "Automatic generation of streaming processor circuit", December 2007, Motorola Corp.

P9. **US Patent 7,073,041**, Malcolm Dwyer, Nikolaos Bellas. "Virtual Memory Translation Unit for Media Acceleration", July 2006, Motorola Corp.

P10. **US Patent 6,868,123** Nikolaos Bellas, Malcolm Dwyer. "A programmable, high performance Vector array unit used for Real-time Motion Estimation", March 2005, Motorola Corp.

P11. **US Patent Application 2006/0159339** Sek M. Chai, Mohamed Ahmed, Nikos Bellas, Greg Kujawa, King F. Lee, Abelardo Lopez Lagunas. "Method and apparatus as pertains to captured image statistics ".

P12. **US Patent Application 2006/0262140** Greg Kujawa, Mohamed Ahmed , Nikos Bellas, Sek M. Chai , King F. Lee, Abelardo Lopez Lagunas. "Method and apparatus to facilitate visual augmentation of perceived reality".

P13. **US Patent Application 2008/0120497** Sek M. Chai, Nikos Bellas, Malcolm Dwyer, Dan Linzmeier. "Automated configuration of a processing system using decoupled memory access and computation"

Awards and Honors

June 2000: IEEE Transactions on VLSI. Special issue on the most significant advances in techniques and methodologies for power-conscious design.

Fall 1992: First Rank, Commencement ceremony of School of Engineering , University of Patras, Greece

1988-1992: Greek Scholarship Foundation academic excellence awards for being in the top 5 in the Department of Computer Engineering and Informatics.

Professional Activities

Commitees

- Technical reviewer for Motorola Labs patent committee
- Guest editor. Special issue on embedded computer vision. Journal on Computer Vision and Image Understanding.
- General Chair for the Embedded Computer Vision Workshop, October 2009
- Program Chair for the Embedded Computer Vision Workshop, June 2008
- Member of TPC for the Embedded Computer Vision Workshop 2007, 2008, 2009
- Member of TPC for the International Conference on Microarchitecture (Micro), December 2007
- Publications chair for the International Conference on Microarchitecture (Micro), December 2007

Reviewer

- Technical reviewer for:
  ACM Transactions on Design Automation of Electronic Systems (TODAES)
  IEEE Transactions on Computers (TCOMP)
  IEEE Transactions on VLSI Systems (TVLSI)
  IEEE Transactions on Computer-Aided Design (TCAD)
  Microelectronics Journal, Circuits and Systems
  Design Automation Conference (DAC)
  International Symposium on Microarchitecture (MICRO)
  International Conference on Supercomputing (ICS)

International Symposium on Low Power Electronics and Design (ISLPED)
International Symposium on Computer Architecture (ISCA)
IEEE Workshop on Embedded Computer Vision

Affiliations

- Member of IEEE
- Member of Technical Chamber of Greece

Advising

Muhsen Owaida: Architectural Synthesis using Parallel Programming Models (PhD 2012)

Konstantinos Parasyris: System software techniques to enhance reliability of modern platforms.

Teaching Experience

University of Thessaly: CE658 : Advanced Computer Architecture (Fall 2007)
CE435 : Embedded Systems (Spring 2008-2014)
CE538 : Parallel Computer Architecture (Fall 2008-2011)
CE134 : Introduction to Computer Organization and Design I (Spring 2009-2013)
CE232 : Introduction to Computer Organization and Design II (Fall 2013, 2014, 2015)

Northwestern University: Fully developed a graduate course on Advanced Topics in Computer Architecture in collaboration with professor Gokhan Memik of Northwestern University. The proposal has been approved by the Curriculum Committee of the department of Electrical and Computer Engineering.

Funding

1. **Project Title:** A Universal Micro-Server Ecosystem by Exceeding the Energy and Performance Scaling Boundaries (UniServer).
   Role: Primary Investigator.
   Source of funding: Low power computing, H2020-ICT-2015
   Budget and dates: Total project budget 4.8 million €. Our budget 405,000 €. 2016-2019

2. **Project Title:** Significance-Based Computing for Reliability and Power Optimization (SCoRPiO).
   Role: Coordinator.
   Source of funding: FET-Open Programme, FP7-ICT-2011-C
   Budget and dates: Total budget 1.9 million €. Our budget 420,000 €. 2013-2016

3. **Project Title:** System Software for Future, Heterogeneous, Accelerator-Based Systems (Centaurus)
   Role: Primary Investigator.
   Source of funding: Greek Ministry of Education, Lifelong Learning and Religious Affairs, Aristeia II Program
   Budget and dates: Total budget 250,000 €, July 2014–November 2015

4. **Project Title:** Advanced Mathematical Methods and Software Platform for solving Multiphysics, Multi-

Domain Problems on Modern Computer Architectures: Application to Environmental Engineering and Medical Problems (MATENVMED).
Role: Primary Investigator.
Source of funding: Greek Ministry of Education, Lifelong Learning and Religious Affairs, Thales Program, grant ID: 137
Budget and dates: Total budget 600,000 €, July 2012–November 2015

5. **Project Title:** Automatic Hardware Generation Using the Streaming Paradigm**.**
   Role: Coordinator.
   Source of funding: Marie Curie International Reintegration Grant (IRG), FP7
   Budget and dates: 100,000 € (November 2008-November 2012)

6. **Project Title:** Low Power Microprocessor Design
   Role: Coordinator.
   Source of funding: Intel Corp.
   Budget and dates: $45,000 per year for 3 years (1996-1998)

Citizenship

Greek and US citizenship